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Transmitter Receiver Ip Cores
User Guide

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LVDS SERDES Transmitter /
Receiver IP Cores User Guide
The Video LVDS SerDes
Transmitter / Receiver IP
Core simplifies the design
of video LVDS interfaces,
improves data integrity and
timing margins. For example,
the Transmitter has the
ability to generate a LVDS
transmit clock synchronous
to the video data stream
thereby eliminating the need
to fine-tune a PLL to the
outputted LVDS data.

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Solved: LVDS video serdes IP Core - Community Forums
The LVDS_SERDES IP Core is a high-speed LVDS Transmitter/Receiver pair suitable for a wide range of serial interface applications.

LVDS SERDES RECEIVER
"The Microtronix Video LVDS SerDes Transmitter / Receiver IP Core not only simplifies the design of video LVDS interfaces, it improves data integrity and timing margins" said Philippe Morin, VP Sales & Marketing.

SERDES Transmitter/Receiver (ALTLVDS) Megafunction User

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The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is the possible use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low

Video LVDS SerDes
Transmitter-Receiver IP Core
1. LVDS SERDES
Transmitter/Receiver IP
Cores User Guide The low-
voltage differential
signaling serializer or

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deserializer (LVDS SERDES) IP cores (ALTLVDS_TX and ALTLVDS_RX) implement the LVDS SERDES interfaces to transmit and receive high-speed differential data. You can configure the features of these IP cores using the IP Catalog and parameter editor.

SN65LVDS93B 10 MHz - 85 MHz
LVDS Serdes Transmitter |
TI.com
SERDES Transmitter/Receiver
(ALTLVDS) Megafunction User
Guide November 2007 Features
Features The altlvds
megafunctions implement
either an LVDS deserializer
receiver or an LVDS
serializer transmitter and

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offer many additional features: Parameterizable data channel widths
Parameterizable serializer/deserializer (SERDES) factors

Microtronix Announces Video LVDS SerDes IP Core for HDTV

...

Low-voltage differential signaling, or LVDS, also known as TIA/EIA-644, is a technical standard that specifies electrical characteristics of a differential, serial communication protocol. LVDS operates at low power and can run at very high speeds using inexpensive twisted-pair copper cables.

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Microtronix Video LVDS
SerDes Transmitter /
Receiver IP Core
The LVDS_TX is CMOS
differential line
transmitter designed for
applications requiring ultra
low power dissipation, low
noise, and high data rates.
The devices are designed to
support data rates in excess
of 800 Mbps (400 MHz)
utilizing Low Voltage
Differential Swing (LVDS)
technology ...

LVDS SERDES
Transmitter/Receiver IP
Cores User www.altera.com
You can configure each LVDS
SERDES IP core channel as a

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receiver or a transmitter for a single differential I/O. Each LVDS SERDES IP core channel contains a SERDES, a bitslip block, DPA circuitry for all modes, a high-speed clock tree (LVDS clock tree) and forwarded clock signal for

LVDS SERDES Transmitter / Receiver IP Cores User Guide
The Microtronix Video LVDS SerDes Transmitter / Receiver IP Core provides a complete, easy-to-use Serializer/Deserializer (SerDes) solution to interface a wide variety of video host systems to Flat Panel displays. The core simplifies the design of

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video LVDS interfaces,
improves data integrity and
timing margins.

High-speed LVDS (SERDES)
Transceiver Rev. 1
The Microtronix Video LVDS
SerDes Transmitter /
Receiver IP-Core provides a
complete, easy-to-use
solution to interface with a
wide variety of video host
systems and flat panel
displays. The core
simplifies the design of
video LVDS interfaces,
improves data

High-Speed LVDS (SERDES)
Transceiver IP Core
The low-voltage differential
signaling serializer or

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deserializer (LVDS SERDES)
megafunction IP cores
(ALTLVDS_TX and ALTLVDS_RX)
implement the LVDS SERDES
interfaces to transmit and
receive high-speed
differential data.

LVDS SERDES Intel FPGA IP
User Guide
SERDES Transmitter/Receiver
(ALTLVDS) Megafunction User
Guide Software Version: 8.1
... As design complexities
increase, use of vendor-
specific Intellectual
Property (IP) ... For the
LVDS transmitter and
receiver, the ALTLVDS
megafunction implements
serialization and

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(LVDS SERDES) IP cores
(ALTLVDS_TX and ALTLVDS_RX)
implement the LVDS SERDES
interfaces to transmit and
receive high-speed differen?
tial data.

SERDES Transmitter/Receiver
(ALTLVDS) Megafunction User
Guide

Solved: Hi, Is there Video
LVDS serdes
transmitter/Receiver IP core

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is available in Xilinx? If
so Please share the details.

LVDS Transmitter IP Core - Design And Reuse

The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the users. The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input and the possible use of the shutdown/clear (SHTDN) signal.

Lvds Serdes Transmitter

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Receiver Ip

The low-voltage differential signaling serializer or deserializer (LVDS SERDES) IP cores (ALTLVDS_TX and ALTLVDS_RX) implement the LVDS SERDES interfaces to transmit and receive high-speed differential data. You can configure the features of these IP cores using the IP Catalog and parameter editor.

Video LVDS SerDes

Transmitter / Receiver IP Core

High-speed LVDS (SERDES) transceiver with up to 8 serial data lanes, generic data width and integrated asynchronous FIFO. Ideal for

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standard LVDS links such as Channel-link[®], Camera-link[®], FPD-link[®], FlatLink[®], MIPI etc. Capable of data rates of up to 500 Mbits/s per lane on basic FPGA devices and 1 Gbits/s+ on higher-end FPGAs.

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